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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/735,374

12/12/2003

Betty Shu Mercer

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23494 7590 09/29/2008  
TEXAS INSTRUMENTS INCORPORATED  
P O BOX 655474, M/S 3999  
DALLAS, TX 75265

EXAMINER

ANDUJAR, LEONARDO

ART UNIT

PAPER NUMBER

2826

NOTIFICATION DATE

DELIVERY MODE

09/29/2008

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/735,374	MERCER ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 9/08/2008.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1,7,16,17,19-21,23 and 33-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,7,16,17,19-21,23 and 33-3 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/11/2008 has been entered.

### ***Election/Restrictions***

2. Applicant's election without traverse of claims 1-3, 7, 16, 17 and 19-23 in the reply filed on 06/27/2006 is acknowledged.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

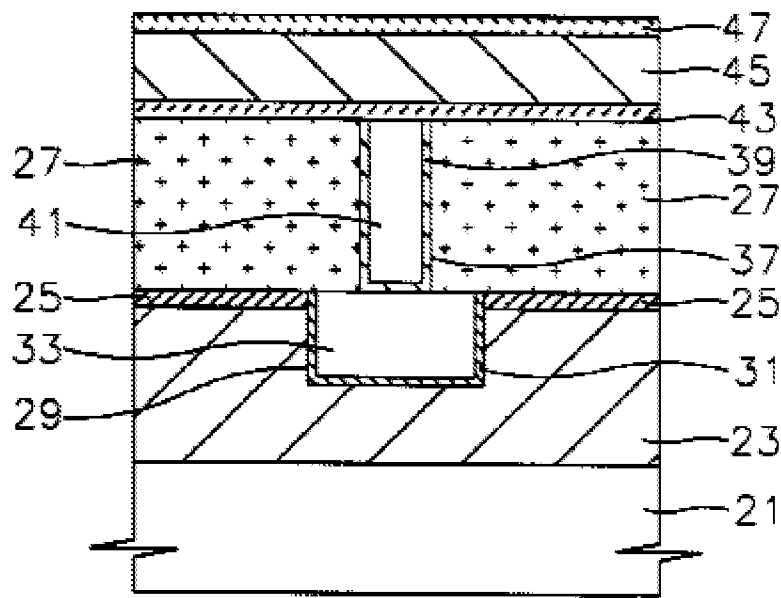
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 7, 33, 34 and 38 rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,545,358) in view of Thomas et al. (US 5,117,276) further in view of Sung et al. (US 6,171,927) further in view of Shih (US 5,827,782).

5. Regarding claim 1, Jeong (e.g. fig. 2) shows an integrated circuit, comprising: a semiconductor substrate 21 comprising device elements and one or more metallization layers interconnecting the device elements and having an uppermost layer 23/33

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comprising metal regions 33 (e.g. tungsten); a protective overcoat 27 formed over the metallization layers, the protective overcoat having vias 37 through it; a conductive barrier layer 39 conformal to the via, a bottom surface of the conductive barrier abutting at least one of the metal regions; tungsten plugs 41 substantially filling the vias; and thick copper 45 formed over the protective overcoat and forming connections to the tungsten plugs (clm. 1 and 18).



Although it is well known in the art that the uppermost layer (i.e. Jeong's 23) include multiple metal regions disposed between dielectric regions Jeong does not explicitly show it, nor the material selection for overcoat 27 (inter layer insulating). Also, it is not disclosed that the metal regions can be made of aluminum. However, Thomas (e.g. fig. 1K) shows an uppermost layer comprised by metal regions 108 disposed between dielectric regions (14, 15 & 30). Shih teaches that silicon oxynitride and silicon nitride are suitable materials for making interlayer insulating (see claim 3). Sung

teaches that plug can be made of tungsten or aluminum (col. 9/lis. 1-11). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the uppermost layer disclosed by Jeong having multiple metal regions disposed between dielectric regions as suggested by Thomas to interconnect the plurality of electrical device formed on the semiconductor device, to make the protective overcoat of Jeong in view of Thomas of silicon oxynitride or silicon nitride due to their relative high dielectric constant and cost and to use aluminum instead of tungsten to make the metal regions 33 to simplify the process and to reduce cost. Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. Moreover, the claim would have been obvious to because a particular known technique was recognized as part of the ordinary capabilities of one skilled in the art see *KSR International Co. v. Teleflex Inc.*, 550 U.S., 82 USPQ2d 1385(2007). In this case, silicon oxynitride, silicon nitride and aluminum are standard materials for interlayer dielectric layers and contact plug respectively.

6. Regarding claims 7, Jeong teaches that the thick copper forms interconnections between device elements within the integrated circuit (col. 1/lis. 55-62).

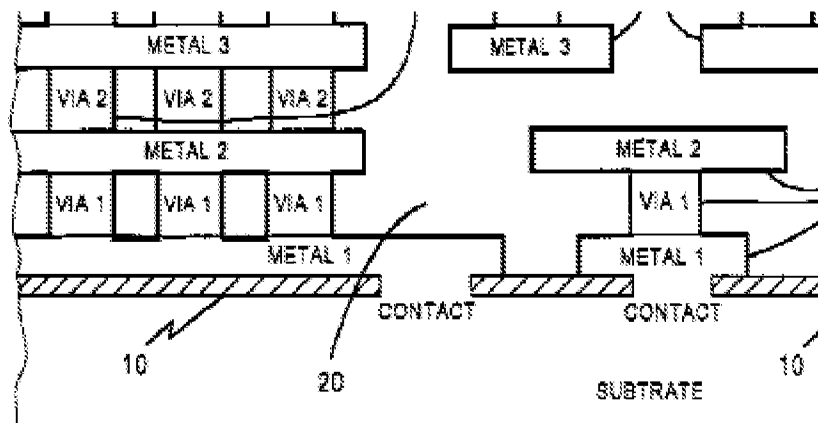
7. Regarding claim 33, Jeong in view of Thomas in view of Sung further in view of Shih show that the tungsten plug is electrically couple at least one of the thick copper connections to one of the metal regions.

8. Regarding claim 34, Jeong in view of Thomas further in view of Sung further in view of Shih shows that the thick copper substantially overlies at least one of the metal regions.

9. Regarding claim 38, Jeong teaches a copper seed layer 43 formed directly onto the surface of each of the tungsten plugs, wherein the copper seed layer comprises a conductive barrier (e.g. TiN) layer to prevent copper from diffusing into the protective overcoat (col. 3/lls. 66-67 & col. 4/ll. 1).

10. Claims 16, 19-21, 23 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,545,358) in view of Buynoski (US 6,218,282) further in view of Shih (US 5,827,782).

11. Regarding claims 16 and 20, Jeong (e.g. fig. 3) shows an integrated circuit, comprising: a semiconductor substrate 21 comprising device elements and one or more metallization layers interconnecting the device elements and having an uppermost layer 23-51 comprising pads; a protective overcoat 27 formed over the metallization layers, the protective overcoat having vias 37 through it; wherein the array of vias are formed over individual bond pads, tungsten plugs 41 substantially filling the vias and connecting to the uppermost layer bond pads; and thick copper 45 formed over the protective overcoat and forming connections to the tungsten plugs (clm. 1 and 18). Jeong does not teach that multiple vias are formed over individual bond pad or the material for making the protective overcoat 27. Nonetheless, Buynoski (e.g. fig. 4) shows an integrated circuit having multiple vias 1 formed over individual bond pads (metal 1).



Shih teaches that silicon oxynitride and silicon nitride are suitable materials for making interlayer insulating (see claim 3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form multiple vias over individual bond pads disclosed by Jeong as suggested by Buynoski to increase device density and performance, and to make the protective overcoat of Jeong in view of Buynoski of silicon oxynitride or silicon nitride due to their relative high dielectric constant and cost. Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. Moreover, the claim would have been obvious to because a particular known technique was recognized as part of the ordinary capabilities of one skilled in the art see *KSR International Co. v. Teleflex Inc.*, 550 U.S., 82 USPQ2d 1385(2007). In this case, silicon oxynitride or silicon nitride are standard materials for interlayer dielectric layers.

12. Regarding claim 19, Jeong teaches that the plug is made of tungsten with have a coefficient of thermal expansion less than or equal to about 8 ppm/C.

13. Regarding claim 21, Jeong teaches that the uppermost layer is an aluminum metallization (col.3/lis. 9-10).

14. Regarding claim 23, Jeong teaches that the thick copper forms interconnections between device elements within the integrated circuit (col. 1/lis. 55-62).

15. Regarding claim 36, Jeong in view of Buynoski shows that the multiple metal plugs individually couple the thick copper connection to the bond pads.

16. Claim 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,545,358) in view of Buynoski (US 6,218,282) further in view of Shih (US 5,827,782) further in view of Ting et al. (US 5,969,422).

17. Regarding claim 17, Jeong in view of Buyoski further in view Shih discloses the claimed invention except for a plug made of copper. Ting teaches that copper is a suitable material for contact plugs (abstract, col. 6/lis. 10-15)). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the contact plug disclosed by Jeon in view of Buynoski of copper as suggested by Ting, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

18. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,545,358) in view of Thomas et al. (US 5,117,276) further in view of further in view of Sung et al. (US 6,171,927) further in view of Sung et al. (US 6,171,927) further in view of Shin (US 5,827,782) further in view of Or-Bach et al. (US 6,476,493).



19. Regarding claim 35, Jeong in view of Thomas further in view of Sung further in view of Shih teaches most aspects of the instant invention including a thick copper but does not explicitly teaches that the thick copper layer does not extend over at least a portion of the dielectric region. However, it is implicitly disclosed because metal interconnections are arranged as grid type array. Therefore, it is not possible for a layer to overlay the whole surface of the integrated circuit unless the layer is a metal plane. For example Or-Barch (e.g. fig. 3) shows the different interconnection metal levels interconnected by vias wherein an upper layer does not extend over the dielectric regions of a lower level (i.e. the space defined by at least two metal layers in the same level). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the thick copper layer such as to do not extend over at least a portion of the dielectric region disclosed by Jeong in view of Thomas further in view of Sung further in view of Shih to provide an interconnection system which has minimal parasitic capacitance and it is mechanically strong.

20. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,545,358) in view of Thomas et al. (US 5,117,276) further in view of further in view of Sung et al. (US 6,171,927) further in view of Shih (US 5,827,782) further in view of Forouhi et al. (US 5,272,101).

21. Regarding claim 37, Jeong teaches a conductive barrier layer 43 formed over and conformal to the protective overcoat, wherein the barrier layer comprises titanium-nitride (TiN, col. 3/lls. 66-67 & col. 4/ll. 1) but does not disclose that TiW is a suitable material for barriers. Nevertheless, Forouhi teaches that TiN and TiW are suitable

materials for barriers (col. 10/lls. 21-22). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the barrier of TiW instead of TiN as suggested by Forouhi because TiW is a suitable material to improve the adhesion of a subsequent metal layer. Moreover, the claim would have been obvious to because a particular known technique was recognized as part of the ordinary capabilities of one skilled in the art see *KSR International Co. v. Teleflex Inc.*, 550 U.S., 82 USPQ2d 1385(2007). Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

### ***Response to Arguments***

22. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

23. Applicant argues that Jeong fails to disclose a pad. However, a contact areas (contact areas of the plug 37) disclosed by Jeong can be recognized as a pad. Although the applicant uses terms different to those of the prior art to label the claimed invention, this does not result in any structural difference between the claimed invention and the prior art. The use of different terminology to describe the plurality of elements that constitute an integrated circuit as this is just a writing style and the way in which a structural limitation is expressed does not affect the configuration of the described elements.

***Conclusion***

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

26. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leonardo Andújar/  
Primary Examiner, Art Unit 2826

September 24, 2008